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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,694	09/23/2003	Anthony Ciancio	SC12836ZP	2205

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EXAMINER	
MANDALA, VICTOR A	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,694	CIANCIO ET AL.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,204,069 Summerfelt et al.

1. Referring to claim 1, a semiconductor device comprising: a semiconductor substrate, (Figure 10 #30), a first electrode, (Figure 10 #50 "W Col. 6 Line 62" & 42 "TiN Col. 6 Line 22"), formed over the semiconductor substrate, (Figure 10 #30); a first conductive smoothing layer, (Figure 10 #34 "TiO Col. 5 Line 38), formed over the first electrode, (Figure 10 #50 & 42), wherein the first conductive smoothing layer, (Figure 10 #34), has a surface roughness less than, (It is inherent that TiO layer has a smaller atomic size than the W layer, thus being smoother), that of the first electrode, (Figure 10 #50 & 42); a dielectric layer, (Figure 10 #36), formed on the first conductive smoothing layer, (Figure 10 #34); and a second electrode, (Figure 10 #46), formed over the dielectric layer, (Figure 10 #36).

2. Referring to claim 2, a semiconductor device, further comprising: a second conductive smoothing layer, (Figure 10 #38 "TiN Col. 5 Line 65), formed between the dielectric layer, (Figure 10 #36) and the second electrode, (Figure 10 #46), wherein the second conductive smoothing layer, (Figure 10 #38), has a roughness less than, (It is inherent that TiN layer has a

smaller atomic size than the W layer, thus being smoother), that of the second electrode, (Figure 10 #46).

3. Referring to claim 3, a semiconductor device, wherein the second conductive smoothing layer comprises a refractory metal, (Figure 10 #38 "TiN Col. 5 Line 65).

4. Referring to claim 4, semiconductor device, wherein the first electrode comprises a first layer comprising a metal, (Figure 10 #50), and a second layer comprising a refractory nitride, (Figure 10 #42), and the second electrode comprises a metal, (Figure 10 #46).

5. Referring to claim 5, a semiconductor device, wherein the first electrode, (Figure 10 #50 Col. 6 Line 65), and the second electrode comprise a refractory nitride, (Figure 10 #46 Col 6 Line 42).

6. Referring to claim 6, a semiconductor device, wherein the refractory nitride comprises a material selected from the group consisting of titanium nitride and tantalum nitride, (Figure 10 #50 Col. 6 Line 65 and Figure 10 #46 Col 6 Line 42).

7. Referring to claim 7, a semiconductor device, wherein the first conductive smoothing layer comprises titanium, (Figure 10 #34 "TiO Col. 5 Line 38").

8. Referring to claim 8, a semiconductor device, wherein the dielectric layer comprises a high dielectric constant material, (Figure 10 #36 Col. 5 Line 43).

9. Referring to claim 9, a semiconductor device, wherein the first electrode, the first conductive smoothing layer, the dielectric layer and the second electrode are part of a metal-insulator-metal (MIM) capacitor, (Figure 10).

10. Referring to claim 10, a semiconductor device, further comprising: a capping layer, (Figure 10 #42 "TiN Col. 6 Line 22"), over the first electrode, (Figure 10 #50 "W Col. 6 Line

62"), wherein the capping layer comprises a refractory nitride, (Figure 10 #42 & 42 "TiN Col. 6 Line 22"), and the first electrode comprises a metal, (Figure 10 #50 "W Col. 6 Line 62").

11. Referring to claim 11, a semiconductor device comprising: a conductive layer, (Figure 10 #50 "W Col. 6 Line 62" & 42 "TiN Col. 6 Line 22"), a smoothing layer, (Figure 10 #34 "TiO Col. 5 Line 38), formed in contact with the conductive layer, (Figure 10 #50 & 42), wherein the smoothing layer, (Figure 29 #34), has a surface roughness less than, (It is inherent that TiO layer has a smaller atomic size than the W layer, thus being smoother), that of the conductive layer, (Figure 29 #50 & 42); and a dielectric layer, (Figure 10 #36), formed in contact with the smoothing layer, (Figure 10 #34).

12. Referring to claim 12, a semiconductor device, wherein the conductive layer comprises a metal, (Figure 10 #50 "W Col. 6 Line 62").

13. Referring to claim 13, a semiconductor device, wherein the conductive layer comprises titanium nitride, (Figure 10 #42 "TiN Col. 6 Line 22"), and the smoothing layer comprises titanium, (Figure 10 #34 "TiO Col. 5 Line 38).

14. Referring to claim 14, a semiconductor device, wherein the conductive layer, the smoothing layer and the dielectric layer are part of a device selected from the group consisting of a transistor and a capacitor, (Col. 1 Lines 18-22 & Col. 3 Line 5-9).

15. Referring to claim 15, a semiconductor device, wherein the conductive layer comprises a first layer comprising a metal and a second layer comprising a refractory nitride, (Figure 10 #50 "W Col. 6 Line 62" & 42 "TiN Col. 6 Line 22").

16. Referring to 16, a semiconductor device, wherein the dielectric layer is a high dielectric constant material, (Figure 10 #36 Col. 5 Line 43).

17. Referring to claim 17, a semiconductor device comprising: a semiconductor substrate, (Figure 10 #30), a first electrode, (Figure 10 #50 "W Col. 6 Line 62" & 42 "TiN Col. 6 Line 22"), formed over the semiconductor substrate, (Figure 10 #30), wherein the first electrode, (Figure 10 #50 & 42), comprises a first layer comprising metal, (Figure 10 #50 "W Col. 6 Line 62"), and a second layer over the first layer, wherein the second layer comprises a refractory nitride, (Figure 10 #42 "TiN Col. 6 Line 22"); a first smoothing layer, (Figure 10 #34 "TiO Col. 5 Line 38), formed over the first electrode, (Figure 10 #50 & 32), wherein the first smoothing layer comprises a refractory metal, (Figure 10 #34 "TiO Col. 5 Line 38); a dielectric layer, (Figure 10 #36), formed on the first smoothing layer, (Figure 10 #34); and a second electrode, (Figure 10 #38 "TiN Col. 5 Line 65" & 46 "W Col. 6 Line 38"), formed over the dielectric layer, (Figure 10 #36), wherein the second electrode, (Figure 10 #38 "TiN Col. 5 Line 65" & 46 "W Col. 6 Line 38"), comprises a third layer comprising a refractory nitride, (Figure 10 #38 "TiN Col. 5 Line 65"), and a fourth layer over the third layer, wherein the fourth layer comprises a metal, (Figure 10 #46 "W Col. 6 Line 38").

18. Referring to claim 18, a semiconductor device, wherein the refractory nitride comprises a material selected from the group consisting of titanium nitride and tantalum nitride, ("TiN Col. 5 Line 65" & "TiN Col. 6 Line 22").

19. Referring to claim 19, a semiconductor device, wherein the refractory metal comprises titanium, ("TiN Col. 5 Line 65" & "TiN Col. 6 Line 22").

20. Referring to claim 20, a method for forming semiconductor device comprising: providing a semiconductor substrate, (Figure 10 #30); forming a first electrode, (Figure 10 #50 "W Col. 6 Line 62" & 42 "TiN Col. 6 Line 22"), formed over the semiconductor substrate, (Figure 10 #30);

forming a first conductive smoothing layer, (Figure 10 #34 "TiO Col. 5 Line 38), formed over the first electrode, (Figure 10 #50 & 42), wherein the first smoothing layer, (Figure 10 #34), has a surface roughness less than, (It is inherent that TiO layer has a smaller atomic size than the W layer, thus being smoother), that of the first electrode, (Figure 10 #50 & 42); forming a dielectric layer, (Figure 10 #36), formed on the first smoothing layer, (Figure 10 #34); and forming a second electrode, (Figure 10 #38 "TiN Col. 5 Line 65" & 46 "W Col. 6 Line 38"), formed over the dielectric layer, (Figure 10 #36).

NATHAN J FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 28

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
11/22/04